FIBERBLAZE
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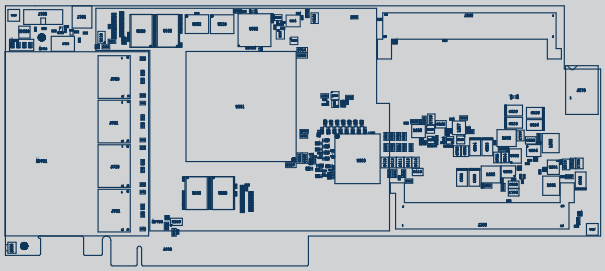

fbC2CGg3 supporting the fbCapture framework

The Fiberblaze fb2CGg3 offers 2x100GE network connectivity and line rate capture to host memory with zero packet loss and hardware packet processing.
The fbC2CGg3 card is based on cutting edge Xilinx FPGA technology, providing packet filtering, advanced processing, traffic management, load balancing and host offloading mechanisms. This high performance hardware platform connects to 100GE using QSFP28 modules and performs packet processing, while delivering a sustained throughput to host memory of up to 224 Gbps. The use of QSFP28 cages also allows use of QSFP to support 8x10GE, 2x40GE as wells as 8x25GE.
The card uses a single-slot PCIe solution through a 16-lane PCIe slot. It also features a second PCIe connector for cable connection to a second PCIe slot. The second PCIe connector can also serve as a card-to-card interconnect path to a second card. Both use cases enable effective traffic management and load balancing in NUMA environments.
This card is also available as a cost optimized variant for 10GE and 40GE.

NETWORK INTERFACE

- IEEE standard: IEEE 802.3 10GE, 40GE, 25GE, 100GE
- Physical interface: 2 x QSFP28 port
- 10GE and 25GE supported through break-out cable assemblies
- Supported QSFP28 modules (25GE/100GE)
  - SR4, LR4, PSM4, CWDM4/CLR4, CR4 (DAC), ER4
  - Appropriate 4x25GE Break-out modules
- Supported QSFP+ modules (10GE/40GE)
  - SR4, LR4, PSM4/IR4, CWDM4, ER4, ZR4 BiDi (850 nm) CR4 (DAC)
  - Appropriate 4x10GE Break-out modules
- Ethernet PHY directly embedded in FPGA

HOST INTERFACE

- Physical bus connector: 16 lane PCIe
- PCIe bus type: 16 lanes PCIe Gen3
  - Cost optimized 10/40GE variant support 12 lanes
- Optional 2nd PCIe cable connect
  - Extra 2x8 lanes via bifurcation
  - Card interconnect (release TBD)
- PCIe compliant
- 64 logical channels that can be connected to DMA or egressed to physical output ports

ON BOARD MEMORY

- On board buffering for application robustness
- 16 GB 64 bit DDR4

PERFORMANCE

- Capture rate (bursts): Line rate
- Capture rate (sustained): Line rate
- Transmission rate (selective bypass): Line rate
- Transmission rate (daisy chain): Line rate

LATENCY

- Less than 3.2 µs to host memory
- Less than 3.2 µs from host memory to Tx
- Non-blocking sending, allowing user applications to operate independently

TIME STAMPING AND SYNC

- Resolution = 3.2 ns
- Accuracy down to 20 ns
- Daisy chain PPS between multiple cards supported
  - Via COAX or Card interconnect adapter
- PPS synchronization via SMA connector
- Optional PTP IEEE 1588-2008 RJ45 via secondary supporting card

CONFIGURATION

- Dual boot images with automatic fallback to fail-safe image
- Full firmware upgrades via supplied tools or fbCAPTURE API

ENVIRONMENT

- Physical dimensions: ¾ length, standard height
- PCIe: 111 x 254 mm
- Weight: 320g
- Operating temperature: 0 – 55°C, 30 – 130°F
- Operating humidity: 20 – 80%
- Hardware compliance: RoHS, CE
- Passive cooling, with adequate host cooling
- Active cooling solution available

ADDITIONAL BOARD SUPPORT

- fbCAPTURE API
- On-board temperature sensor
- On-board multi-color status LED
- Link and Activity LED for ports

CARD VARIANTS

- All card variants have FPGAs optimized for resource requirements of the varying link types.
  Available models:
- fbC2CGg3 for 10/40/25/100GE
- fbC2CGg3-2x40 for 40GE, cost optimized
- fbC2CGg3-8x10 for 10GE, cost optimized
- Mixed speed models can can be customized

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Dedication to Performance

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The fbCAPTURE Framework

The fbCAPTURE framework is a combination of FPGA firmware and a software API in C that utilizes the full potential present in a range of FPGA based network interface cards from Fiberblaze. The fbCAPTURE Cards are designed with a combination of a powerful FPGA and large amounts of high speed onboard memory to ensure zero packet loss even at line rate performance. The fbCapture API is common for all the capture cards for 1GE, 10GE, 40GE and 100GE line rates. This simplifies system integration greatly, as support for multiple network rates can be achieved with the same integration efforts.

SOFTWARE API

- Same API for all Fiberblaze capture cards
- WinPCAP and LibPCAP compatibility
- C based API (DLL/Shared library)
- Linux, Windows & FreeBSD
- Multi Direct Memory Access streaming using to Packet Ring Buffers (PRB)
- Up to 64 channels to host controlled PRBs
- 255 channels for traffic redirection
- User error handlers
- No additional SW library dependencies

SERVER LOAD BALANCING

- Host server traffic load balancing supported
- Up to 64 channels to multiple host processes' memory
- Selective traffic redirection
- Load balancing to external hosts via optical Tx interfaces
- Dual level load balancing. Hosts & CPUs
- Copy same PDU to multiple channels
- Distribution without CPU overhead using 2, 3, 5 and N tuple hashing or filter rules

SUPPORTED HARDWARE

- Fiberblaze cards for 1, 10, 40 and 100 Gbit/s using pluggable transceiver modules (SFP, SFP+, QSFP+, CFP4, QSFP 28)
- Ethernet PHY embedded in FPGA for full packet control
- PCIe Gen1, Gen2 and Gen3 support for optimal host throughput
- Monitoring via SPAN port/optical splitters
- Ethernet auto-negotiation
- Limitless Daisy Chaining of monitored optical fibers between cards, at full signal strength, reducing number tapping of points
- Board to board interconnect for data merge and redirection

FILTERS

- A wide range of inline filters can be defined and combined in real-time to meet a variety of filtering requirements on a wide range of protocol header parameters
- On-the-fly reconfiguration of filters
- Filter types available include ranges, pattern match, fixed/dynamic offset and value, bit masks and value, true/false, not, hash values, compounds and more on e.g.:
- Link layer:
  ARP, Tunnels (L2TP), MAC, VLAN incl. Stacked VLAN, MPLS, etc.
- Internet layer:
  IPv4, Ipv6, ICMP, RIP, OSPF, ECN, etc.
- Transport layer:
  UDP, TCP, SCTP, etc.
- Application layer:
  HTTP, FTP, LDAP, POP, RTP, SIP, SMTP, Telnet, GTPv1, GTPv2, RNSAP and RANAP via SIGTRAN, GTP-U payload headers etc.
- Option to allow on-wire error packets through
- Optional on-wire error and undersized frames to processing

PACKET SLICING

- A wide range of slicing rules can be applied to conserve memory and storage by truncating packets
- Fixed length slicing
- Dynamic slicing where truncation may start from any specified header and include user definable number of bytes thereafter

PACKET DESCRIPTOR

- Captured packets can be enriched with descriptors generated by the adapter at line rate.
- PCAP Descriptor
- Standard Descriptor
- Multiple Extended Descriptor
- Multiple time formats supported

PACKET PROCESSING

- Host acceleration of protocol parsing
- Zero copy PDU handling
- Packet layers indexing of protocol layers
- No protocol parsing needed for access to individual layers
- Optional insertion of alignment ticks (packets) in host memory buffer every 100ms
- Optimized packet transfers for batch processing

DEDUPLICATION

- Removal of duplicated packets
- Configurable duplication detection parameters

IP DEFRAGMENTATION

- IP fragments are correlated on-the-fly and processed as the initial fragment of the original packet
- Correlated fragment handling ensures that all related fragments are delivered to same channel as specified for the complete original packet
- True representation of on-wire packets

NETWORK STATISTICS

- Elaborated subset of RFC2819 RMON1
- Statistics each second for each interface
- Counters for special purpose firmwares
- Network counters include: number of octets, CRC align errors, undersize packets, oversize packets incl. Jumbo frames, packet size distribution & more
- Provided via API or via supplied independent Fiberblaze application

ON BOARD SENSOR READINGS

- Temperature with preset minimum, maximum card operating temperature
- Optical signal level readings
- Link status
- Provided via API or via supplied independent Fiberblaze application